Parallel Integrated Circuit Test Apparatus and Test Method

ABSTRACT

A test apparatus (300) comprising a single handler (304) is coupled to a first tester (336) and second tester (308). A first test procedure is performed on a set of second IC's using the first tester (336), simultaneously while a second test procedure is performed on a first set of IC's using the second tester (308). Sets of IC's are tested sequentially, in parallel, by a plurality of testers (336/308) within a single handler (304).